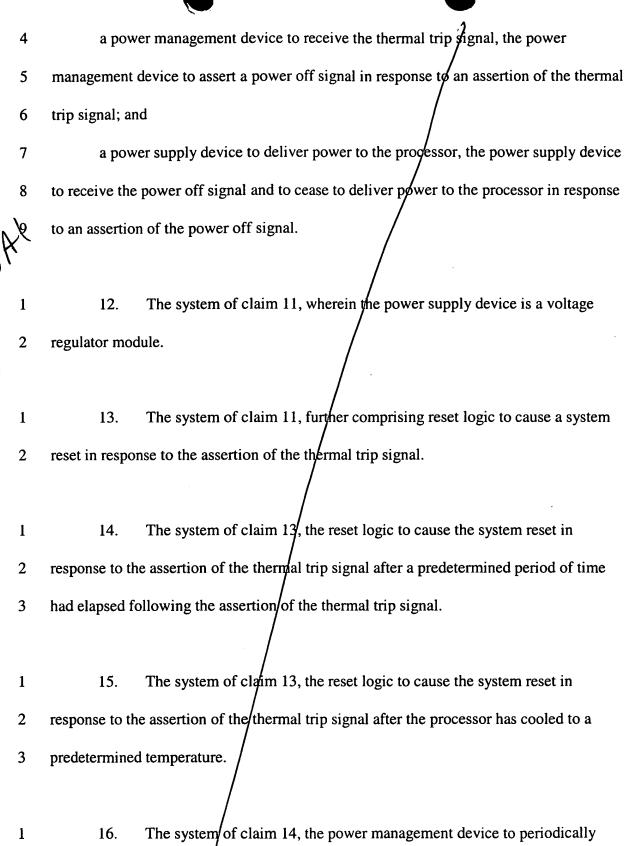## CLAIMS

What is claimed is:

1   1.   A method, comprising:

2   detecting that a processor is overheated, and

3   automatically removing power from the processor.

1   2.   The method of claim 1, further comprising rebooting a computer system,

2   the computer system including the processor.

1   3.   The method of claim 2, further comprising throttling the processor

2   following the reboot.

1   4.   The method of claim 2, further comprising applying a reduced voltage to

2   the processor during and subsequent to the reboot.

1   5.   The method of claim 3, wherein rebooting the computer system includes

2   rebooting the computer system after a predetermined period of time following the

3   detection of the overheated condition.

1   6.   The method of claim 3, wherein rebooting the computer system includes

2   rebooting the computer system after the processor has cooled to a predetermined

3   temperature.

1   7.   The method of claim 3, further comprising:

2   detecting for a second time that the processor is overheated;

3   automatically removing power from the processor for a second time; and

4   again rebooting the computer system.

1   8.   An apparatus, comprising:

2   a processor interface unit to monitor a thermal trip signal from a processor; and

3   a voltage regulator module interface to assert a power off signal to a voltage

4   regulator module in response to an assertion of the thermal trip signal.

1   9.   The apparatus of claim 8, wherein the processor interface periodically

2   asserts a stop clock signal to the processor in response to a system reboot following the

3   assertion of the thermal trip signal.

1   10.   The apparatus of claim 9, further including a status bit that is set in

2   response to the assertion of the thermal trip signal, the status bit to indicate that the

3   system reboot is in response to the assertion of the thermal trip signal.

1   11.   A system, comprising:

2   a processor including a thermal trip signal output that is asserted in response to an

3   overheat condition;

4   a power management device to receive the thermal trip signal, the power

5   management device to assert a power off signal in response to an assertion of the thermal

6   trip signal; and

7   a power supply device to deliver power to the processor, the power supply device

8   to receive the power off signal and to cease to deliver power to the processor in response

9   to an assertion of the power off signal.

1   12.   The system of claim 11, wherein the power supply device is a voltage

2   regulator module.

1   13.   The system of claim 11, further comprising reset logic to cause a system

2   reset in response to the assertion of the thermal trip signal.

1   14.   The system of claim 13, the reset logic to cause the system reset in

2   response to the assertion of the thermal trip signal after a predetermined period of time

3   had elapsed following the assertion of the thermal trip signal.

1   15.   The system of claim 13, the reset logic to cause the system reset in

2   response to the assertion of the thermal trip signal after the processor has cooled to a

3   predetermined temperature.

1   16.   The system of claim 14, the power management device to periodically

2   assert a stop clock signal to the processor during and following the system reset.